AMMENDMENTS TO THE SPECIFICATION

Please replace the Title of the Invention with the following rewritten Title.

"Microprocessor Capable of Native Bit-Field Operations"

Please strike the final four sentences from paragraph 37:

[0037] The mask generator 410 generates a mask field to be used by the execution unit 420 using the begin and end field bit positions. The mask field defines an operand field within the operand to be operated by an operation performed by the execution unit 420. The operand field has a field length delimited by the begin and end field bit positions. The operand field may be contiguous or non-contiguous. The begin and end field bit positions are provided in the field specifier 270 (FIG. 2) of the instruction, or from some special- purpose registers, or from any other sources as discussed earlier. The mask field has a word size equal to the word size of the normal operands used by the execution unit 420. In one embodiment, the mask field is defined by logical 1's, i.e., the bits 1 of the mask field indicate the bit positions of the operands to be operated upon. The bits 0's of the mask field indicate that the corresponding bits of the operand remains unchanged. The mask field essentially defines the portions outside and inside the field to be operated upon. ~~The portion outside the field may remain unchanged or modified (e.g., zero or sign extended). The mask field may or may not be contiguous. In other words, there may be holes within the field. An example of a non-contiguous mask field is 0001 1110 0111 0000 for a 16-bit operand. In other words, the mask generator 410 may generate multiple sub mask fields.~~

Please remove paragraph 50 altogether:

[0050] ~~In addition, the decoders 510 and 520 may decode multiple begin and end bit positions to implement non-contiguous mask field.~~